In the Specification

Please amend the third paragraph on page 2, line 11, as follows:

--One of the main limitations [[on]] of integrated circuit design is heat generation within the integrated circuit, since if the integrated circuit overheats, it may fail to operate properly. It would therefore be advantageous to provide ways of mounting integrated circuits on substrates such that heat is more easily transmitted from them.--

Please amend the fourth paragraph on page 2, line 19, as follows:

--The present invention aims to provide [[a]] new and useful semiconductor packages (that is, substrates incorporating at least one integrated circuit mounted thereon), and methods for mounting integrated circuits on substrates.--

Please amend the second paragraph on page 3, line 5, as follows:

--The plate is preferably shaped so as [[to]] not to block the areas at which the pads of the integrated circuit are connected to the substrate. For example the plate may extend out from under the integrated circuit in directions which are diagonal relative to the overall square or rectangular circumference of the integrated circuit, since the integrated circuit will not generally require wire bonding to the substrate in these directions.--

Please amend the last paragraph beginning on page 5, line 22, as follows:

--Turning to Fig. 3 the structure of Fig. 2 is shown in an exploded view, with the plate 1 taking the form shown in Fig. 1. In this view the pads 35 on the upper surface of the layer 13 are visible, with their corresponding via holes 36. Note that when the plate 1 rests on the substrate 11, the diagonal arms

7 tend not to cover any of these pads 35. The lateral arms 5 do however cover some of the pads 5. For this reason the lateral arms 5 may be omitted. Alternatively, if the lateral arms 5 are included, the die 27 may be designed such that its pads which correspond in position to the position of these arms ([[i.e.]] i.e., its pads at the [[centre]] center of its sides) are the pads which are to be connected to ground. In this case, these pads may be connected directly to the plate 1 rather than to pads on the substrate 11.--

Please amend the first paragraph on page 6, line 4, as follows:

--Note that it is preferred that the rim portion 9 of the device 1 (i. e. the portion of the device 1 which entirely encircles the die 27) is laterally outward of the edge of the substrate 11. This is because the upper surface of the substrate 11 may include a number of areas (such as via holes) having a function which would be disrupted if they were connected to ground. Since the rim 9 is laterally outward of the substrate, the area at which the substrate 11 and plate 1 contact each other is [[minimised]] minimized.--

Please amend the second paragraph on page 6, line 12, as follows:

--The order of steps used to form the arrangement of Fig. 3 is as follows. Firstly, after bumping, the flipchip 22 is located on the substrate 11. Then, the underfill layer 25 is applied. Then the plate 1 is attached to the flipchip 22 by heat-conductive glue. Then the die 27 is attached to the plate 1 by heat-conductive glue. To avoid pressure of the die 27 upon the flipchip 22 the flipchip 22 should be larger in area than the die 27, and this feature also has advantages in terms of the10 count of the two devices. Then the wire-bonding is done to connect the substrate 11 and the die 27. Once [[wirebonding]] wire-bonding is complete[[d]], the resin 31 is applied. As shown in Figs. 2 and 3 the resin 31 is only applied to a central region of the substrate 11 (using a [[mould]] mold, not shown), however the plate 1 can itself constitute the [[mould]] mold and in this case the resin might extend laterally as far as the rim 9.

Alternatively, another rim might be formed on the plate 1 laterally inward of the rim 9 to provide the sides of a mould in which the resin 31 could be formed. Curing of the resin 31 is performed only once to avoid die crack. The marking is done to complete the packaging.

Please amend the first paragraph on page 7 as follows:

--The second embodiment of the invention is shown with reference to Figs 4 to 6. The second embodiment relates to a LFBGAS (low profile ball grid array package) with a fine ball pitch (0.5, 0.65 or 1.00mm). Such BGA packages, delivering higher performance and thermal dissipation, are shrinking in size, so that packaging such silicon dies [[in]] is an increasing challenge.